IN THE CLAIMS

This listing of claims replaces all prior listings:

1. (currently amended) A solid-state imaging device ~~having~~ comprising an imaging region section provided with a plurality of pixels and a processing circuit section for processing an image signal output from the imaging region section, wherein:

each pixel has a photoelectric converting element which generates a signal charge commensurate with a light-receiving amount;

each pixel has a charge holding region of a ~~second~~ conductivity type which holds a signal charge;

each pixel has a transfer transistor, coupled to one side of the photoelectric converting element and the charge holding region, which transfers a signal charge generated by the photoelectric converting element to the charge holding region and has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the photoelectric converting element;

each pixel has a drain transistor, coupled to another side of the photoelectric converting element and a drain line, which drains a signal charge generated by the photoelectric converting element and has a threshold channel potential for turning on the drain transistor which is set to a value higher than [[a]]the potential which depletes the photoelectric converting element;

the solid-state imaging device ~~also~~ includes a driver configuration unit which controls the transfer of signal charges in said device; and

the driver configuration unit sets both [[a]]the threshold channel potential on the turned-on drain transistor[[s]] and [[a]]the threshold channel potential on the turned-on transfer transistor[[s]] higher than the potential which depletes the photoelectric converting element[[s]], wherein a gate potential of the drain transistor is set higher than a gate potential of the transfer transistor.

2. (previously presented) A solid-state imaging device according to claim 1, wherein each pixel has a reset transistor for resetting the charge holding region with a signal charge, an amplifying transistor for outputting an electric signal corresponding to a

potential on the charge holding region, and a selecting transistor for selectively activating the amplifying transistor.

3. (canceled)

4. (previously presented) A solid-state imaging device according to claim 1, configured so that after simultaneously resetting at least one floating diffusion part on all the pixels in the imaging region section, signal charges of the photodiodes on all the pixels are simultaneously transferred to the charge holding regions, next the signal charges transferred to the charge holding regions are read out on a pixel-row basis, to keep the drain transistor on until the reading operation proceeds to a predetermined exposure start row and drain the signal charges of the photodiodes on all the pixels, and to turn off the drain transistor when proceeded to the predetermined exposure start row and start an exposure on all the pixels.

5. (previously presented) A solid-state imaging device according to claim 4, configured so that, for each pixel the photodiode, immediately after transferring the signal charge of the photodiode to the charge holding region by the transfer transistor, has remaining charges of 20 or less while the photodiode, immediately after draining the signal charge of the photodiode by the drain transistor, has remaining charges of 20 or less.

6. (cancelled)

7. (previously presented) A solid-state imaging device according to claim 4, wherein, for each pixel the drain transistor being on has a gate voltage level higher than a power voltage of a digital circuit mounted on the solid-state imaging device.

8. (previously presented) A solid-state imaging device according to claim 4, wherein, for each pixel the drain transistor is off during an operation to read out the

signal charge of the charge holding region on a pixel row preceding to the exposure start row.

9. (previously presented) A solid-state imaging device according to claim 2, wherein, for each pixel the transfer transistor, the reset transistor and the amplifying transistor have respective gate wirings provided in a direction along the pixel row, to be driven on a pixel-row basis and the drain transistor has a gate wiring provided in a direction along the pixel column, the drain transistor gate wiring being short-circuited common between all the pixels at an outside of the imaging region section.

10-15. (canceled)

16. (currently amended) A camera apparatus for outputting an image taken by a solid-state imaging device, the camera apparatus comprising the solid-state imaging device having an imaging region section provided with a plurality of pixels and a processing circuit section for processing an image signal outputted from the imaging region section,

wherein,

each pixel has a photoelectric converting element which generates a signal charge commensurate with a light-receiving amount;

each pixel has a transfer transistor which transfers a signal charge generated by the photoelectric converting element to the charge holding region and has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the photoelectric converting element;

each pixel has a drain transistor which drains a signal charge generated by the photoelectric converting element and has a threshold channel potential for turning on the drain transistor which is set to a value higher than [[a]]the potential which depletes the photoelectric converting element;

each pixel has a charge storing region formed by a ~~second~~ conductivity type impurity layer in a layer beneath a charge separating region which holds a signal charge;

the solid-state imaging device ~~also~~ includes a driver configuration unit which controls the transfer of signal charges in said device; and

the driver configuration unit sets both [[a]]the threshold channel potential on the turned-on drain transistor[[s]] and [[a]]the threshold channel potential on the turned-on transfer transistor[[s]] higher than the potential which depletes the photoelectric converting element[[s]], wherein a gate potential of the drain transistor is set higher than a gate potential of the transfer transistor.

17. (previously presented) A camera apparatus according to claim 16, wherein, for each pixel the solid-state imaging device further has a reset transistor for resetting the charge holding region with a signal charge, an amplifying transistor for outputting an electric signal corresponding to a potential on the charge holding region, and a selecting transistor for selectively activating the amplifying transistor.

18. (canceled)

19. (previously presented) A camera apparatus according to claim 16, wherein, in the solid-state imaging device, after simultaneously resetting the charge holding regions on all the pixels in the imaging region section, signal charges of the photodiodes on all the pixels are simultaneously transferred to the charge holding regions, next the signal charges transferred to the charge holding regions are read out on a pixel-row basis, to keep the drain transistor on until the reading operation proceeds to a predetermined exposure start row and drain the signal charges of the photodiodes on all the pixels, and to turn off the drain transistor when proceeded to the predetermined exposure start row and start an exposure on all the pixels.

20. (previously presented) A camera apparatus according to claim 19, wherein, in the solid-state imaging device, for each pixel the photodiode, immediately after transferring the signal charge of the photodiode to the charge holding region by the transfer transistor, has remaining charges of 20 or less while the photodiode, immediately

after draining the signal charge of the photodiode by the drain transistor, has remaining charges of 20 or less.

21. (cancelled).

22. (previously presented) A camera apparatus according to claim 19, wherein, in the solid-state imaging device, for each pixel the drain transistor being on has a gate voltage level higher than a power voltage of a digital circuit mounted on the solid-state imaging device.

23. (previously presented) A camera apparatus according to claim 19, wherein, in the solid-state imaging device, for each pixel the drain transistor is off during an operation to read out the signal charge of the charge holding region on a pixel row preceding to the exposure start row.

24. (previously presented) A camera apparatus according to claim 17, wherein, in the solid-state imaging device, for each pixel the transfer transistor, the reset transistor and the amplifying transistor have respective gate wirings provided in a direction along the pixel row, to be driven on a pixel-row basis and the drain transistor has a gate wiring provided in a direction along the pixel column, the drain transistor gate wiring being short-circuited common between all the pixels at an outside of the imaging region section.

25. (previously presented) A camera apparatus according to claim 16, further having switch means for switching a shutter operation of the solid-state imaging device between a focal-plane shutter operation and an all-the-pixel simultaneous shutter operation.

26. (original) A camera apparatus according to claim 19, further having exposure time selecting means for selecting an exposure time of the solid-state imaging

device and exposure start row selecting means for selecting the predetermined exposure start row depending upon an exposure time selected by the exposure time selecting means.

27. (currently amended) A solid-state imaging device comprising:

a plurality of pixels each pixel having (a) a light-receiving part, (b) a transfer transistor which reads out a charge generated in the light-receiving part and has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the light-receiving part, (c) a drain transistor which drains the charge generated in the light-receiving part and has a threshold channel potential for turning on the drain transistor which is set to a value higher than [[a]]the potential which depletes the light receiving part, and (d) a charge holding region of a ~~second~~ conductivity type which holds a signal charge; and

a driver configuration unit which controls the transfer of signal charges in said device,

wherein,

the driver configuration unit sets both [[a]]the threshold channel potential on the turned-on drain transistor[[s]] and [[a]]the threshold channel potential on the turned-on transfer transistor[[s]] higher than the potential which depletes the light-receiving part[[s]], wherein a gate potential of the drain transistor is set higher than a gate potential of the transfer transistor.

28. (original) A solid-state imaging device according to claim 27, wherein the charge storing region when substantially depleted includes charges (electrons or charges) in the number of 20 or less.

29. (currently amended) A solid-state imaging device according to claim 27, wherein

each pixel further has a charge holding part for holding a charge read out by the transfer transistor,

the charges stored in the charge storing regions are read out, simultaneously on all the pixels, to the charge holding parts by the transfer transistors,

the charges held at the charge holding parts of the plurality of pixels are read out as pixel signals in a predetermined order, and

the plurality of pixels, in a time period which the pixel signals are read out, are drained of unwanted charges in the charge storing regions by the drain transistors, thereby starting an exposure time period.

30. (currently amended) A solid-state imaging device comprising:

a plurality of pixels, each pixel having (a) a light-receiving part, (b) a transfer transistor which reads out a charge in a manner substantially depleting a charge storing region included in the light-receiving part which has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the light-receiving part, (c) a drain transistor which has a threshold channel potential for turning on the drain transistor which is set to a value higher than [[a]] the potential which depletes the light-receiving part, and (d) a charge holding region of a ~~second~~ conductivity type which holds a signal charge; and

a driver configuration unit which controls the transfer of signal charges in said device, [[,]]

wherein,

the driver configuration unit sets both [[a]] the threshold channel potential on the turned-on drain transistor[[s]] and [[a]] the threshold channel potential on the turned-on transfer transistor[[s]] higher than the potential which depletes the light-receiving part[[s]], wherein a gate potential of the drain transistor is set higher than a gate potential of the transfer transistor.

31. (original) A solid-state imaging device according to claim 30, wherein the charge storing region when substantially depleted includes charges (electrons or charges) in the number of 20 or less.

32. (currently amended) A solid-state imaging device ~~having~~ comprising an imaging region section provided with a plurality of pixels and a processing circuit section for processing an image signal outputted from the imaging region section, wherein,

each pixel has a photoelectric converting element for generating a signal charge commensurate with a light-receiving amount;

each pixel has a charge holding region of a ~~second~~ conductivity type which holds a signal charge;

each pixel has a transfer transistor which transfers a signal charge generated by the photoelectric converting element to the charge holding region and has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the light-receiving part;

each pixel has a drain transistor which drains a signal charge generated by the photoelectric converting element and has a threshold channel potential for turning on the drain transistor which is set to a value higher than [[a]] the potential which depletes the light-receiving part;

each pixel has a reset transistor which resets the charge holding region with a signal charge, an amplifying transistor which outputs an electric signal corresponding to a potential on the charge holding region, and a selecting transistor which selectively activates the amplifying transistor;

the solid-state imaging device also includes a driver configuration unit which controls the transfer of signal charges in said device;

the driver configuration unit sets both [[a]] the threshold channel potential on the turned-on drain transistor[[s]] and [[a]] the threshold channel potential on the turned-on transfer transistor[[s]] higher than the potential which depletes the light-receiving part[[s]], wherein a gate potential of the drain transistor is set higher than a gate potential of the transfer transistor; and

the solid-state imaging device is configured so that after simultaneously resetting the charge holding regions on all the pixels in the imaging region section, signal charges of the photodiodes on all the pixels are simultaneously transferred to the charge holding regions, next the signal charges transferred to the charge holding regions are read out on a pixel-row basis, to keep the drain transistor on until the reading operation proceeds to a predetermined exposure start row and drain the signal charges of the photodiodes on all the pixels.

33. (currently amended) A solid-state imaging device having an imaging region section provided with a plurality of pixels and a processing circuit section for processing an image signal outputted from the imaging region section, wherein,:

each pixel has a photoelectric converting element which generates a signal charge commensurate with a light-receiving amount;

each pixel has a charge holding region of a ~~second~~ conductivity type which holds a signal charge;

each pixel has a transfer transistor which transfers a signal charge generated by the photoelectric converting element to the charge holding region and has a threshold channel potential for turning on the transfer transistor which is set to a value higher than a potential which depletes the light-receiving part;

each pixel has a drain transistor which drains a signal charge generated by the photoelectric converting element and has a threshold channel potential for turning on the drain transistor which is set to a value higher than a potential which depletes the light-receiving part;

each pixel has a reset transistor which resets the charge holding region with a signal charge, an amplifying transistor which outputs an electric signal corresponding to a potential on the charge holding region, and a selecting transistor which selectively activates the amplifying transistor;

the solid-state imaging device also includes a driver configuration unit which controls the transfer of signal charges in said device;

the driver configuration unit sets both [[a]] the threshold channel potential on the turned-on drain transistor[[s]] and [[a]] the threshold channel potential on the turned-on transfer transistor[[s]] higher than the potential which depletes the light-receiving part[[s]], wherein a gate potential of the drain transistor is set higher than a gate potential of the transfer transistor;

the solid-state imaging device is configured so that after simultaneously resetting the charge holding regions on all the pixels in the imaging region section, signal charges of the photodiodes on all the pixels are simultaneously transferred to the charge holding regions, next the signal charges transferred to the charge holding regions are read out on a pixel-row basis, to keep the drain transistor on until the reading operation proceeds to a

predetermined exposure start row and drain the signal charges of the photodiodes on all the pixels; and

for each pixel, the drain transistor is off during an operation to read out the signal charge of the charge holding region on a pixel row preceding to the exposure start row.